IN THE CLAIMS

Claim 1 (currently amended): A CMOS analog multiplexer circuit comprising:

multiple series ~~n-channel/~~p-channel MOS transistor input switches;

multiple series ~~n-channel/~~p-channel MOS transistor output switches;

multiple pull-down n-channel MOS transistor switches; wherein

said circuit prevents cross-signal feed-through from unselected inputs by shunting said feed-through to circuit ground.

Claim 2 (currently amended): The CMOS analog multiplexer circuit of Claim 1 further comprising:

the input of a first series input ~~n-channel/~~p-channel MOS transistor switch coupled to the first circuit input signal;

the input of a second series input ~~n-channel/~~p-channel MOS transistor switch coupled to the second circuit input signal;

the input of a nth series input ~~n-channel/~~p-channel MOS transistor switch coupled to the nth circuit input signal;

the output of said first series input n-channel/p-channel MOS transistor switch coupled to the input of a first output ~~n-channel/~~p-channel MOS transistor switch and to the drain of a first n-channel MOS pull-down transistor;

the output of said second series input n-channel/p-channel MOS transistor switch coupled to the input of a second output ~~n-channel/~~p-channel MOS transistor switch and to the drain of a second n-channel MOS pull-down transistor;

the output of said nth series input n-channel/p-channel MOS transistor switch coupled to the input of a nth output ~~n-channel/~~p-channel MOS transistor switch and to the drain of a nth n-channel MOS pull-down transistor;

the outputs of said first, second, and nth output n-channel/p-channel MOS transistor switches coupled together and to circuit output;

the sources of said first, second, and nth n-channel MOS pull-down transistors coupled to circuit ground;

the gates of all said series input and output ~~n-channel~~ p-channel MOS transistor switches coupled to a logic control signal;

the gates of all said series input and output p-channel MOS transistor switches and all n-channel MOS pull-down transistors coupled to a logic control signal which is the complement of said input/output transistor logic control signal.

Claim 3 (original): The CMOS analog multiplexer circuit of Claim 2, further comprising MOS transistor layouts which have an even number of circuit fingers: wherein

said MOS transistor's parasitic capacitance is reduced by more than 50%; and

said MOS transistor's bandwidth is at least doubled.

Claim 4 (original): The CMOS transistor layout of Claim 3 further comprising:

a CMOS transistor whose architecture has the source and gate split in half such that it consists of the sequence: one-half source, one-half gate, drain, one-half gate, and one-half source;

said CMOS transistor whose drain capacitance is half that of a conventional CMOS transistor;

said CMOS transistor whose gate is split into two parts each having a width of w/2;

said CMOS transistor whose source is split into two parts each having a width of w/2;

said two gate parts coupled together and to transistor gate output;

said two source parts coupled together and to transistor source output.